

APPLICATION  
FOR  
UNITED STATES PATENT APPLICATION  
Entitled  
INTELLIGENT POWER SYSTEM

Inventor(s):

Boris S. Jacobson  
&  
Jacqueline M. Bourgeois

Daly, Crowley & Mofford, LLP  
275 Turnpike Street, Suite 101  
Canton, Massachusetts 02021-2310  
Telephone (781) 401-9988  
Facsimile (781) 401-9966

Express Mail Label No. ER333130117US

## TITLE

Intelligent Power System

## CROSS REFERENCE TO RELATED APPLICATIONS

5           This application claims the benefit of provisional application serial number 60/423,640 filed November 4, 2002, the disclosure of which is hereby incorporated by reference.

## STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH

10           Not Applicable.

## FIELD OF THE INVENTION

          The present invention relates generally to power systems and more particularly to a system which can detect and isolate failed segments and reconfigure the system to  
15   restore power.

## BACKGROUND OF THE INVENTION

          Conventional power distribution systems typically include multiple power sources and storage elements and are known by those of reasonable skill in the art. Despite the  
20   relative simplicity and wide acceptance of this conventional power distribution architecture, the conventional architecture suffers from several disadvantages. With few exceptions, unregulated energy sources are incompatible with parallel connection to a common bus. One problem of the conventional approach is that the architecture requires power regulators to interface incompatible sources to the bus. If such unregulated  
25   sources such as batteries are connected to the common bus, the unregulated source with the highest voltage will back-feed other sources thereby generating circulating currents. The magnitude of these currents depends on the voltage difference between the various sources and the total resistance of the current path. Because the source and bus resistances are low, the circulating currents will degrade system efficiency and may even  
30   damage components and wiring.

Another problem associated with this power system architecture is its susceptibility to single point failures. If the common bus, the load, or the output of a single voltage regulator is shorted, the whole system can be disabled. Still another problem associated with conventional power system architectures is the systems inability to control the power flow. Because there is only one bus that connects all loads and all power sources, this architecture does not allow delivering power to a section of the load from selected sources. The conventional architecture lacks flexibility, i.e., failed elements or bus segments cannot be isolated and disconnected from the system.

## 10 SUMMARY OF THE INVENTION

An intelligent power system is presented. The system includes one or more common power sources and one or more subsystem components interconnected with the common power sources. Each common power source includes a regulated bus, an unregulated bus, a sensor, a controller and a plurality of switches operated by the controller. A subsystem component includes a regulated bus, an unregulated bus, a power source, a sensor, a controller and a plurality of switches operated by the controller. With such a configuration, the system is able detect and isolate failed segments of the power system and is reconfigurable to restore power.

## 20 BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be more fully understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

Figure 1 is a block diagram of a conventional power system;

Figure 2 is a block diagram of the power architecture of the present invention;

Figure 3 is a block diagram of a common source element of the present invention;

Figure 4 is a block diagram of a subsystem element of the present invention;

Figure 5 is a block diagram of a single unregulated source embodiment of the present architecture;

Figure 6 is a block diagram of a three-regulator embodiment of the present invention;

Figure 7A is a block diagram of a time-shared embodiment of the present architecture;

Figure 7B is a timing diagram of the time-shared embodiment of Figure 7A;

Figure 8 is a block diagram showing an arrangement wherein three subsystems  
5 are operating from a single regulator in the time-shared mode;

Figure 9 is a timing diagram showing the time-shared mode of operation;

Figure 10 is a graph showing output voltage versus output current for a regulator of the present power system;

Figure 11A is a block diagram showing an arrangement wherein two subsystems  
10 are operating from a single power source;

Figure 11B is a timing diagram showing power delivery for the arrangement of Figure 11A;

Figure 12A is a block diagram showing another arrangement wherein two subsystems are operating from a single power source;

Figure 12B is a timing diagram showing power delivery for the arrangement of  
15 Figure 12A;

Figure 13A is a block diagram showing an arrangement having multiple faults;  
and

Figure 13B is a timing diagram showing power delivery for the arrangement of  
20 Figure 13A.

## DETAILED DESCRIPTION OF THE INVENTION

The present invention comprises a new power system architecture that resolves the problems associated with conventional power systems and further provides important  
25 advantages not available with conventional power system architectures. Autonomous power systems have to satisfy conflicting requirements such as high density, low weight and volume, energy storage, continuous and reliable operation with partial damage, fault isolation and self-generating and restoring capabilities.

30 Referring now to Figure 1, a prior art power system architecture 1 is shown. This architecture 1 uses individual voltage regulators 10a – 10N to couple multiple power

sources 20a – 20N to a common regulated bus 30. The regulated bus 30 is used to provide power to one or more loads 40a-40N. The regulators can be realized as voltage source regulators 10a – 10N to couple voltage sources 20a – 20N to the regulated bus 30, and also as storage regulators 50a – 50N to couple storage sources 60a – 60N to the regulated bus 30.

Referring now to Figure 2, a high-level block diagram of the presently disclosed power system 100 is presented. This architecture comprises a common power source and  $m*n$  interconnected subsystems 120. The number of connections between subsystems 120 and the common power source 110 may vary from zero (a self-sufficient system) to  $m*n$  (a source-dependent system). Each line between a subsystem 120 and the common power source 110 represents multiple power and signal connections. The number of interconnections between subsystems may vary from zero (a completely independent system) to  $m*n - 1$  (a fully connected system). Each line between subsystems 120 in Figure 2 represents multiple power and signal connections between the subsystems 120. Another version of this architecture includes multiple subsystems wired together and connected to the common power source as groups.

A block diagram of the common power source 110 is shown in Figure 3. The common power source 110 includes an unregulated voltage bus 112, a regulated voltage bus 114, Po power sources 116, Ro regulators 118, So bus stabilizers 111, Eo energy storage units 113, sensors 115 and a controller 117. A power source 110 may be realized as a battery, a generator, a fuel cell, a solar cell or the like. A stabilizer 111 is similar to a regulator in that a stabilizer is a power conversion device wherein one voltage level is converted to another voltage level. An energy storage device 113 may be realized as a battery, flywheel, capacitor, inductor or similar type device. All elements of the common power source except the controller 117 and sensors 115 are connected to one or both buses through controlled switches 119. The switches 119 may be electronic solid state, vacuum tube, or electro-mechanical devices. The output of each regulator 118 is connected to regulated buses of all subsystems as well as the regulated bus 114 of the common source. As an alternative, the common regulated bus 114 may be connected to

one or more regulated buses of individual subsystems. The subsystem-to-subsystem control signals interconnect may be the same interconnect (electrical (wire-based), optical, infrared, RF, etc.) used for interconnecting a subsystem controller to a power source controller, although other embodiments may use a different interconnect for the subsystem-to-subsystem control signals interconnect than the subsystem-to-power source control signals interconnect.

Referring now to Figure 4 a block diagram of a subsystem 120 (subsystem 1,1 of Figure 2 in this example) is shown. The subsystem includes a regulated voltage bus 122, an unregulated voltage bus 123, PR regulated power sources 127 (only one shown in Figure 4), R regulators 126 (only one shown in Figure 4), S bus stabilizers 129, E energy storage units 128 (only one shown in Figure 4), D loads 121, sensors 124 and a subsystem controller 125. All subsystem elements except the controller 125 and sensors 124 are connected to one or both buses through controlled switches 130. Each regulated power source 127 is connected to regulated buses of all other subsystems as well as to the internal regulated bus 122.

The presently disclosed architecture provides several advantages not available from conventional power systems. A system comprising incompatible sources can operate without regulators. One way of achieving this is to activate only a single power source at any moment in time. Another method is to break connections between subsystems that contain power sources using controlled switches and operate all sources simultaneously (completely independent system). The presently disclosed architecture can also use switches to operate power sources in a sequential way or switching between the two modes described above. Thus, the new approach applies to systems that contain both regulated and unregulated buses.

Because the system comprises self-sufficient interconnected subsystems as well as the common power source, the presently disclosed power system is not susceptible to single point failures.

Each subsystem or element of the new system is connected to all other elements and to the common energy source and storage. Controllers can direct power flow from one subsystem to another subsystem, from the central source to any number of subsystems, and from any number of subsystems to storage elements. This control is accomplished by a controller opening and/or closing the appropriate switches to provide the desired configuration. Each controller is in communication with a respective sensor and further each controller is in communication with each other controller.

In the event of a failure, the controllers, by way of the sensors, will detect failed elements or bus segments. The controllers then isolate the failed element or bus segment and re-configure the distribution to restore power by activating and/or deactivating the appropriate switches. Constant monitoring of the power flow through bus segments allows the controller to determine their condition and identify failures. For any waveforms of voltage  $V(t)$  and current  $I(t)$ , the instantaneous power at the output of the power source or at the load fed by a bus segment is expressed as follows:

$$P = 1/T \int V(t) I(t) dt \text{ for the integration time interval from } 0 \text{ to } T$$

This expression can be simplified for specific waveforms. For example, in the case of sinusoidal voltage and current the power is:

$$P_{\text{SINE}} = V_{\text{RMS}} I_{\text{RMS}}$$

One way to identify failed elements or bus segments is to compare the power supplied by a source with the power consumed by a load and voltage at the source with voltage at the load. For example, if a system consists of one source and multiple loads the power balance for lossless distribution is expressed as follows:

$$P_{\text{SOURCE}} = \Sigma(P_{\text{LOAD1}} + P_{\text{LOAD2}} + \dots + P_{\text{LOADG}}), \text{ summing from } 1 \text{ to } G$$

Where

$P_{\text{SOURCE}}$  is power at the source

$P_{\text{LOAD1}}$  through  $P_{\text{LOADG}}$  is power at the load

Assuming that the loads are not regenerative, power at the source always equals to the total power consumed by the loads. If the bus segment feeding one load failed, the power balance equation would not hold. To eliminate the possibility that the load itself failed, the controller would measure the voltage at the load terminals. If the load voltage equals to the source voltage and the load does not draw its share of power, then the load has failed. If the load voltage does not equal to the source voltage (for lossless distribution) and the load does not draw its rated power, then the bus segment has failed.

Referring now to Figure 5, an application involving an unregulated system 200 is shown. The system comprises two subsystems 120a and 120b, and a common power source 110. All power sources in this system are unregulated and are therefore incompatible with parallel operation. For the mode of operation shown in Figure 5, the common power source 110 and source in the subsystem 2 are disconnected and both loads operate from the single power source located in the subsystem 1.

The reliability of the new architecture is based upon the power transfer between components through the interconnect. Because power flows through multiple conductors and the system contains multiple sources, the failure of any single element (or possibly multiple elements) does not disrupt operation of the power system.

Conductor 1 provides power from subsystem 120a to energy storage unit 113 of the common power source 110. Additionally, conductors 2 and 3 provide power from subsystem 120a to energy storage unit 113 of the common power source 110. Conductors 3 and 4 also provide power from subsystem 120a to subsystem 120b unregulated bus 123, load 121b and energy storage device 128. Conductors 1, 2 and 6 also provide power from subsystem 120a to subsystem 120b unregulated bus 123, load 121b and energy storage device 128.

The power source 210 is disconnected from the common bus of Common Power Source 110 by opening switch 211. Similarly, the power source 116b of subsystem 120b is also disconnected from the unregulated bus by opening switch 212 and is further



disconnected from the unregulated bus of subsystem 120a by the opening of switch 213. In order to permit power source 116a of subsystem 120a to provide power to load 121a of subsystem 120a and also to load 121b of subsystem 120b switches 214-218 of subsystem 120a are closed as are switches 219, 219a and 220 of subsystem 120b. Power from power source 116a flows from subsystem 120a to common power source 110 through conductor 1 of the system interconnect. Power from power source 116a also flows from subsystem 120a to subsystem 120b through conductor 3, 4 and 6 of the system interconnect. Power also flows from power source 116a through common power source 110 and to subsystem 120b through conductor 2 of the system interconnect. With such an arrangement power source 116a is able to provide power to load 121a and also to load 121b.

Other modes of operation supported by the present power system architecture include a self-sufficient mode of operation wherein both subsystems are disconnected from each other and the common source, a mode wherein operation is from the common power source, a mode wherein operation is from the power source in the second subsystem, and a time-shared mode of operation wherein some or all of the power sources are turned on sequentially.

Referring now to Figure 6, a power system 300 comprising a common power source 110 feeding two subsystems 120a and 120b is shown. Subsystem 120a includes one main regulator 310 and one redundant regulator 320 with each regulator capable of providing full power for either subsystem 120a or 120b. Figure 6 illustrates one mode of operation when regulator 330 of subsystem 120b has failed and regulator 320 in subsystem 120a continuously provides power to the subsystem 120b.

Switches 340 and 341 of common power source 110 are closed, switches 333 and 334 of subsystem 120a are open while switches 335 through 339 of subsystem 120a are closed. In subsystem 120b, switches 331 and 332 are open while switches 342, 443 and 334 are closed. With this arrangement power from power source 210 of common power source 110 is provided to regulator 310 and regulator 320 of subsystem 120a. The

regulators then provide regulated power to the load 121a of subsystem 120a and to the load 121b of subsystem 120b.

This example demonstrates the ability of the present power system architecture to reduce the total number of regulators to three and maintain redundancy for both subsystems. A conventional solution calls for connecting buses 1 and 2 in parallel, but if the voltage V1 (bus 1) is different from the voltage 2 (bus 2) this approach will not be feasible. In this case, the buses have to be separate and redundant operation of subsystem 2 will require an additional regulator (four total).

Figure 7A shows the same system as Figure 6, but operating under a different set of conditions. This system is labeled 300'. In this example, two of the regulators are out of service (regulators 310 and 330 have failed, while regulator 320 remains operational). As shown in Figure 7A, the power system overcomes these failures by operating on a time-shared basis. As shown in the timing diagram of Figure 7B, regulator 320 feeds the subsystem 120a for time interval T1 and feeds subsystem 120b for time interval T2. This mode does not have to be periodic and controllers can modify both time intervals as required. Similarly to the previous case, if the input voltage for the two subsystems is different, the subsystem 120a controller can vary the output of regulator 330 to satisfy each subsystem's requirements.

In the system 300' switches 340 and 341 of the common power source are closed. In subsystem 102a switches 333, 336 and 338 are opened, switch 339 is closed and switches 334, 335 and 337 are cycled between the open and closed positions. In subsystem 120b, switches 331, 332 and 342 are opened while switches 343 and 344 are cycled. As shown in Figure 7B, power is delivered to subsystem 120a for a predetermined period of time, then to subsystem 120b for a predetermined period of time, and there is no overlap between the power delivery to the two subsystems. Switches 337 and 344 are closed and switches 334, 335 and 343 are opened to provide power to load 121a of subsystem 120a. Switches 337 and 344 are opened and switches 334, 335 and 343 are closed to provide power to load 121b of subsystem 120b. These switches 334,

335, 337, 343 and 344 are cycled in order to provide power on a time-shared basis to subsystem 120a and subsystem 120b.

Figures 8 through 10 illustrate a method of using energy storage devices to feed pulsed loads. Figure 8 shows a configuration 500 including three subsystems 120a, 120b and 120c that operate from a single regulator 510 while three other regulators 520, 530, and 540 are out of service. Also, as shown in graph 600 of Figure 9, loads for subsystems 120a and 120b draw pulsed power that exceeds the rated power of the regulator 510. Even under these demanding conditions, the present power system architecture provides power on a time-shared basis to all loads if the following conditions are met:

Time intervals when one regulator is connected to a given subsystem do not overlap,

$$T \geq \sum T_a \text{ for the summation from } a = 1 \text{ to } a = 3$$

Where  $T_a$  is the time interval when a subsystem is connected to the regulator and  $T$  is the repeatable time interval.

The average power  $P_{reg}$  delivered by the regulator does not exceed the total average power consumed by all loads or, for a lossless system:

$$P_{reg} \geq (1/T) * \int (\sum P_a(t)) dt$$

for the interval of integration from  $t = 0$  to  $t = T$  and the summation from  $a = 1$  to  $a = 3$

Where  $P_a(t)$  is the load power for a given subsystem load,  $a$  is the load number.

The system 500 operates as follows. Because load 511 of subsystem 120a requires more power than regulator 510 can deliver, the energy storage 512 provides the rest of the power. When the load 511 is turned off, the regulator 510 recharges the energy storage 512 during the remainder of the time interval  $T1$ .

When load 513 of subsystem 120b is turned on, the regulator is still connected to the subsystem 120a. Consequently, the energy storage unit 514 is feeding the subsystem 120b until the beginning of time interval  $T2$ . At this time, regulator 510 of subsystem

120a starts delivering power to load 513 and recharging the energy storage 514 of the subsystem 120b.

Subsystem 120c operates in a similar way. The only difference is that subsystem 120c has a constant load thereby its power demand never exceeds the rated power of the regulator 510. During time intervals T1 and T2 the energy storage unit 516 of subsystem 120c provides power to load 515. When regulator 510 is connected to subsystem 120c, it starts recharging the energy storage unit 516 and feeding load 515.

Similar to the previous described configurations, the pulsed load mode does not have to be periodic and controllers can modify all time intervals as needed as long as the conditions listed above are satisfied. Also, if the input voltage needed by subsystems is different, the subsystem controller can vary the output of the regulator to satisfy each system's requirements.

Referring now to Figure 10, a graph 700 showing the different modes of operation of the regulator is shown. The graph 700 shows a first mode of operation referred to as the voltage mode 710. As can be seen in the voltage mode of operation the voltage is nearly constant regardless of the output current. Output voltage versus current (VA) characteristic of the regulators also has constant power mode 720. In this mode the voltage varies directly opposite the current resulting in constant power over a range of voltages and currents. Additionally, the regulators have a constant current mode 730. In this mode the regulator provides a constant current value over a range of voltages. A foldback mode 740 is also shown. In foldback mode the regulator decrease the output current with increasing overload, reaching a minimum at short circuit. This minimizes internal power dissipation under overload conditions.

Referring now to Figure 11A, a system 800 is shown in a configuration wherein two subsystems 120a and 120b operate from a common power source. An additional unregulated power source 810 is incorporated in the subsystem 120a. If the rated power of unregulated power source 810 is sufficient to feed only one subsystem, time-sharing

will allow operating both subsystems 120a and 120b in the event of a failure of the common power source.

Switch 801 of common power source 110 is closed, switch 813 is open and switches 802 and 803 are cycled. In subsystem 120a switches 805, 806 and 808 are closed while switches 807 and 804 are cycled. In subsystem 120b, switch 812 is closed while switches 809 and 811 are cycled. With this arrangement power from power source 810 of subsystem 120a is provided to regulator 820 at one time interval through switch 807. Further, power is delivered from power source 810 of subsystem 120a to regulator 830 of subsystem 120b via switch 804 during a second time interval.

As shown in Figure 11B, during time interval T1 the power source 810 delivers power to the subsystem 120a through the regulator 820 while the regulator 830 is disconnected from the system. As the time interval T2 begins, the regulator 820 is turned off and power starts flowing from power system 810 to the subsystem 120b through the regulator 830. This example shows a case when either load does not exceed the rated power of the source. If this condition is not satisfied, energy sources can be used to average peak power demands of the loads as described above with respect to Figures 8-10.

Figure 12A shows a system 900 in a configuration wherein two subsystems 120a and 120b are fed by a common power source 110. Unlike the system shown in Figure 11A, the power source 910 in this system generates regulated voltage and does not have a connection to the second subsystem 120b. Again, if the common source 920 fails, the power source 910 can feed both subsystems 120a and 120b on a time-shared basis.

Switch 901 of common power source 110 is closed, and switch 902 is open. Switch 904 of subsystem 120a is closed while switches 903 and 905 are cycled. In subsystem 120b, switch 908 is closed and switches 906 and 907 are cycled. With this arrangement power from power source 910 of subsystem 120a is provided to the load of

subsystem 120a through switch 903 during a first time interval and power is delivered to subsystem 120b through switch 905 during a second time interval.

As shown in Figure 12B, during the time interval T1, power source 910 delivers power directly to the subsystem 120a bypassing the regulator 930 that is disconnected via switch 905 from the regulated bus 940 of subsystem 120a. During the time interval T2, the regulator 930 is connected to regulated bus 940 via switch 905 and converts its voltage V1 to the input voltage for the regulator 950 that feeds the second subsystem 120b. This mode of operation is particularly useful when one common source powers several subsystems that have different regulated bus voltages. To enable this mode of operation, the regulator 930 is bi-directional i.e. it is able to send power from the input to the output and vice versa. If either subsystem needs pulsed power, energy sources can be used to average peak power loads as described above.

Referring now to Figure 13A, an embodiment 1000 which demonstrates how the new architecture improves reliability and maintains operation in the presence of multiple faults is presented. In this example, a second failure disabled the regulator 1010, so neither power source 1020 nor regulator 1010 are in service. Under these conditions, the regulated power source 1030 feeds both subsystems 120a and 120b on a time-shared basis while the regulator 1040 is turned off via switch 1007.

Switches 1001 and 1002 of common power source 110 are open. Switch 1006 of subsystem 120a is closed, switch 1007 is open and switches 1003-1005 are cycled. In subsystem 120b, switch 1009 is open and switch 1008 is cycled. With this arrangement power from power source 1030 of subsystem 120a is provided to the load 121a of subsystem 120a via switches 1003 and 1005 during a first time interval and power is delivered to subsystem 120b via switch 1004 during a second time interval.

As shown in Figure 13B, during the time interval T1, the power source 1030 delivers power to the subsystem 120a. During the time interval T2, power source 1030 is switched from bus 1050 with voltage V1 to the bus 1060 with voltage V2. To enable this

mode of operation, the source's output has to be programmable and its range shall include voltage V2. This example shows a case when either load does not exceed the rated power of the power source 1030. If this condition is not met, energy sources can be used to average peak power loads as described above with respect to Figures 8-10.

5

An intelligent power system has been described. The power system includes one or more common power sources and one or more subsystem components interconnected with the common power sources. With such a configuration, the system is able detect and isolate failed segments of the power system and is reconfigurable to restore power.

10

Having described preferred embodiments of the invention it will now become apparent to those of ordinary skill in the art that other embodiments incorporating these concepts may be used. Additionally, the software included as part of the invention may be embodied in a computer program product that includes a computer useable medium.

15

For example, such a computer usable medium can include a readable memory device, such as a hard drive device, a CD-ROM, a DVD-ROM, or a computer diskette, having computer readable program code segments stored thereon. The computer readable medium can also include a communications link, either optical, wired, or wireless, having program code segments carried thereon as digital or analog signals. Accordingly, it is

20

submitted that that the invention should not be limited to the described embodiments but rather should be limited only by the spirit and scope of the appended claims. All publications and references cited herein are expressly incorporated herein by reference in their entirety.